WHAT IS CLAIMED IS:

1. A photodiode comprising:

a well located in a substrate;

a floating node located in the well;

shallow trench isolation (STI) regions located over and laterally opposing the floating node;

a borderless contact buffer layer located over at least the floating node;

a dielectric layer located over the borderless contact buffer layer; and

a borderless contact extending through the dielectric layer and the borderless contact buffer layer to the floating node.

2. The photodiode of Claim 1 wherein the borderless contact buffer layer is selected from the group consisting of: SiON, SiN, and combinations thereof.

3. The photodiode of Claim 1 wherein the dielectric layer is selected from the group consisting of: silicon dioxide, low dielectric material, and combinations thereof.

4. The photodiode of Claim 1 wherein a second refractive index of the borderless contact buffer layer is between a first refractive index of the dielectric layer and a third refractive index of the floating node.

5. The photodiode of Claim 1 wherein the dielectric layer has a first refractive index of between about 1.3 and about 1.5, the borderless contact buffer layer has a second

refractive index of between about 1.8 and about 2.5, and the floating node has a third refractive index of greater than about 3.

6. The photodiode of Claim 1 wherein the well is doped with an n-type impurity and the floating node is doped with an n+ type impurity.

7. A method of manufacturing a photodiode sensor, comprising:

forming a well in a substrate;

forming a shallow trench isolation (STI) element at least partially in the well;

removing a portion of the STI element to form STI regions opposing an exposed portion of the well;

forming a floating node in the exposed portion of the well;

forming a borderless contact buffer layer over at least the floating node and along sidewalls of the STI regions;

forming an interlevel dielectric layer over the borderless contact buffer layer; and

forming a borderless contact extending through the interlevel dielectric layer and the borderless contact buffer layer to the floating node.

8. The method of Claim 7 wherein the borderless contact buffer layer is selected from the group consisting of: SiON, SiN, and combinations thereof.

9. The method of Claim 7 wherein the dielectric layer is selected from the group consisting of: silicon dioxide, low dielectric material, and combinations thereof.

10. The method of Claim 7 wherein a second refractive index of the borderless contact buffer layer is between a first refractive index of the dielectric layer and a third refractive index of the floating node.

11. The method of Claim 7 wherein the dielectric layer has a first refractive index of between about 1.3 and about 1.5, the borderless contact buffer layer has a second

refractive index of between about 1.8 and about 2.5, and the floating node has a third refractive index of greater than about 3.

12. The method of Claim 7 wherein the well is doped with an n-type impurity and the floating node is doped with an n+ type impurity.

13. The method of Claim 7 wherein the floating node is formed by implanting ions through an opening between the opposing STI regions.

14. The method of Claim 7 wherein the portion of the STI element is removed by a dry etching process.

15. The method of Claim 7 further comprising forming a conductive interconnect on the dielectric layer and contacting the borderless contact.

16. A semiconductor device, comprising:

first and second adjacent wells located in a substrate;

a first transistor gate structure located over at least a portion of the first well;

a floating node located in the second well;

shallow trench isolation (STI) regions located over and laterally opposing the floating node;

a borderless contact buffer layer located over at least the floating node and the first transistor gate structure;

a dielectric layer located over the borderless contact buffer layer;

a first borderless contact extending through the dielectric layer and the borderless contact buffer layer to the floating node;

a second borderless contact extending through the dielectric layer and the borderless contact buffer layer to the first transistor gate structure; and

an interconnect located over the dielectric layer and coupling the first and second borderless contacts.

17. The device of Claim 16 wherein the borderless contact buffer layer is selected from the group consisting of: SiON, SiN, and combinations thereof.

18. The device of Claim 16 wherein the dielectric layer is selected from the group consisting of: silicon dioxide, low dielectric material, and combinations thereof.

19. The device of Claim 16 wherein a second refractive index of the borderless contact buffer layer is between a first refractive index of the dielectric layer and a third refractive index of the floating node.

20. The device of Claim 16 wherein the dielectric layer has a first refractive index of between about 1.3 and about 1.5, the borderless contact buffer layer has a second refractive index of between about 1.8 and about 2.5, and the floating node has a third refractive index of greater than about 3.

21. The device of Claim 16 wherein the second well is doped with an n-type impurity and the floating node is doped with an n+ type impurity.

22. The device of Claim 16 wherein the first well is doped with a first impurity type and the second well is doped with a second impurity type opposite to the first impurity type.

23. The device of Claim 16 further comprising: a third well doped with the first impurity type and located adjacent the second well on a side opposite the first well; and a second transistor gate structure located over portions of the second and third wells.